

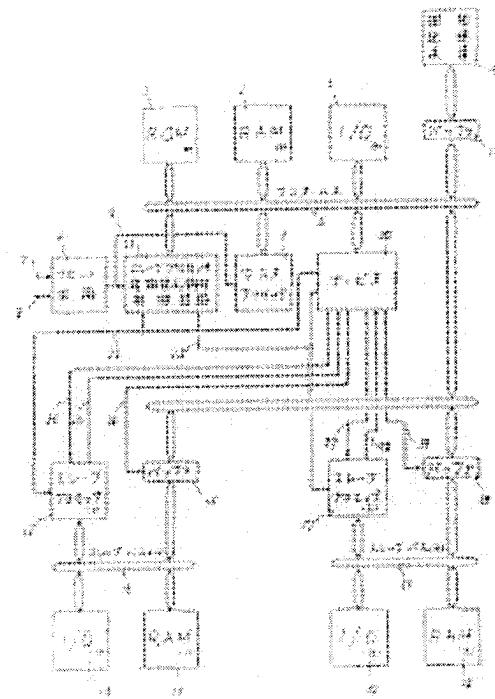
## MULTIPROCESSOR SYSTEM

Bibliographic data	Mosaics	Original document	INPADOC legal status
<b>Publication number:</b>	JP61288262 (A)		
<b>Publication date:</b>	1986-12-18		
<b>Inventor(s):</b>	YOKOTA MASAYUKI +		
<b>Applicant(s):</b>	HITACHI LTD +		
<b>Classification:</b>			
<b>- international:</b>	<i>G06F15/16; G06F15/17; G06F15/177; G06F9/445; G06F15/16; G06F9/445; (IPC1-7): G06F15/16</i>		
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<b>Application number:</b>	JP19850129823 19850617		
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<a href="#">View INPADOC patent family</a>			
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## Abstract of JP 61288262 (A)

Translate this text

PURPOSE: To make a ROM of a slave memory unnecessary to use an overall area as a shared memory by inhibiting start of a slave processor until execution of initial program load (IPL) for the slave processor is completed. CONSTITUTION: When a master processor 1 is started, a microprogram on a ROM m3 as a master memory is started to execute IPL of an IPL program for slave processors (1)12 and (n)17 to a RAM m2, and the master processor 1 executes this program. Thus, pertinent processing programs are initially loaded to slave memories RAM (1)13 and (n)18 from an auxiliary storage device 10. Thereafter, the master processor changes the signal from a control circuit 31 to the permission state, and the slave processor whose start is permitted starts the program processing on the slave memory.



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